In order to anticipate, the reference must identically disclose each claim element. In fact, Tavallaei does not identically disclose many of the recited claim elements.

The office action asserts that component 14 in Figure 2 of Tavallaei corresponds to the recited scaleable node controllers. However, Tavallaei describes component 14 as a local advanced programmable interrupt controller (APIC). A local APIC is not identical to a scaleable node controller.

In the Examiner's response to arguments, at numbered paragraph 53, the Examiner purports to answer applicants' prior traversal, but does so only selectively. Specifically, the Examiner does not answer and apparently concedes applicants' argument that the different terminology in fact describes different structure and functionality. The Examiner does not answer and apparently concedes applicants' argument that every 'controller' does not perform the same function as every other 'controller'. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a node controller performs a different function than an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a node controller has a different structure from an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that a node controller may have suitable structure to participate in an interrupt handling scheme, but an interrupt controller would not have suitable structure to perform the function of controlling a node of a multi-node system.

Applicants understand the Examiner's position to be that because the APIC 14 is a 'controller' and may have some connection to a 'node', it may read on the recited 'node controller'. Applicants submit that this interpretation is an unreasonably broad interpretation of the claim language and an incorrect reading of the reference. As the case appears to be heading for appeal, applicants respectfully request that the Examiner provide a reasoned response to the foregoing arguments in order to reduce issues for appeal. Applicants consider each unanswered argument as conceded for the purposes of appeal.

The office action asserts that component 26 in Figure 2 of Tavallaei corresponds to the recited scalability port switch. However, Tavallaei describes component 26 as an external input / output advanced programmable interrupt controller (I/O APIC). An I/O APIC is not identical to a scalability port switch.

In the Examiner's response to arguments, at numbered paragraph 53, the Examiner purports to answer applicants' prior traversal, but does so only selectively. Specifically, the Examiner does not answer and apparently concedes applicants' argument that the different terminology in fact describes different structure and functionality. The Examiner does not answer and apparently concedes applicants' argument that every 'I/O' controller does not perform the same function as every other I/O switch. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a port switch performs a different function than an I/O interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a port switch has a different structure from an I/O interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that a port switch may have suitable structure to participate in an interrupt handling scheme, but an I/O interrupt controller would not have suitable structure to perform the function of switching ports of a multi-node system. The Examiner does not answer and apparently concedes applicants' argument that in some applications a port switch may include structure to resolve node addresses and that the I/O APIC 26 appears to lack such structure.

Applicants understand the Examiner's position to be that because the I/O APIC 26 may be broadly considered as a 'switch' and may have some connection to a 'port', it may read on the recited 'port switch'. Applicants submit that this interpretation is an unreasonably broad interpretation of the claim language and an incorrect reading of the reference. As the case appears to be heading for appeal, applicants respectfully request that the Examiner provide a reasoned response to the foregoing arguments in order to reduce issues for appeal. Applicants consider each unanswered argument as conceded for the purposes of appeal.

Among other things, claim 1 further recites that the scalability port switch is to determine an address of one of said scaleable node controllers from said interrupt request. Tavallaei fails to teach or suggest this further recitation. In contrast to the present invention, Tavallaei describes a multi-processor system with local APICs 14 connected to the I/O APIC 26 over the APIC bus 16. Tavallaei describes that the I/O APIC 26 generates an interrupt message on the APIC bus 16, which is monitored by all the local APICs 14. The local APICs 14 appear to be responsive to the content of the interrupt messages for passing on local interrupts for the associated processor 12. The Examiner has not identified (and applicants are unable to identify) any portion of Tavallaei that teaches or suggests that the local APICs 14 have addresses associated therewith.

In the Examiner's response to arguments, at numbered paragraph 54, the Examiner appears to be relying on a theory of inherency. In other words, the Examiner appears to be arguing that because the message is received by the appropriate local APIC 14, the local APIC 14 inherently must have an address associated therewith. However, this is incorrect. Any of a number of schemes may be utilized for getting messages to the appropriate processor 12. For example, the processor 12 in Tavallaei may include a processor ID and the message on the APIC bus 16 may include the processor ID. Tavallaei expressly describes that the APIC 26 maintains a table that indicates "which of the processors 12 the interrupt is to be directed." (see col. 7, lines 43-44, emphasis added). The fact of the matter is that Tavallaei is completely silent with respect to any address associated with the local APIC 14. In order to clarify issues for possible appeal, the Examiner should admit that Tavallaei does not expressly teach the recited addresses and set forth the Examiner's position with respect to inherency (particularly the Examiner's technical argument for how such addresses are allegedly the only possible way to deliver data from the I/O APIC 26 to the local APIC 14).

Again, the Examiner only selectively answers applicants' traversal. The only clarification provided by the Examiner is that instead of 'address' the Examiner now relies on 'ID, i.e. address'. The term 'i.e.' means 'that is'. Apparently the Examiner is of the opinion that an ID is identical with an address. This is clear error. To clarify issues for possible appeal, applicants respectfully request that the Examiner either explicitly state that he is

relying on either the ID reading directly on the recited address, if the Examiner is relying on some theory of inherency, or otherwise clarify how the Examiner has analyzed the reference to come to the conclusion that the scheme disclosed in Tavallaei reads on the claim recitations relating to determining an address of the scaleable node controller.

Because Tavallaei fails to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claim 1 is not anticipated by Tavallaei, and is patentable over Tavallaei. Claims 2-3 depend from claim 1 and are likewise patentable.

With respect to claims 9 and 18, for the reasons given above Tavallaei does not disclose the recited scaleable node controller or the recited scalability port switch. Claims 9 and 18 have been amended to clarify that determining the scaleable node controller includes determining an address of the scaleable node controller. For the reasons given above Tavallaei does not disclose determining an address of the local APIC 14. Accordingly, claim 9 and its dependent claims 10-12 and 16-17 are not anticipated by and are patentable over Tavallaei. Likewise, claim 18 and its dependent claims 19-21 and 25-26 are patentable over Tavallaei.

With respect to claims 11 and 20, the office action identifies col. 7 lines 41-44 for the recited comparing a priority of the interrupt request with a priority of the processor. However, the cited portion makes no reference whatsoever to a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Tavallaei.

In the Examiner's response to arguments, at numbered paragraph 55, the Examiner clarifies that the rejection relies on a theory of inherency. MPEP § 2112 sets forth the requirements and burdens the Examiner must meet in order to rely on inherency. The Examiner has not met these burdens. Applicants presume that the Examiner is familiar with the requirements of MPEP § 2112 to sustain a rejection based on inherency and take the Examiner's failure to even attempt to meet these requirements as an admission that the reliance on inherency is misplaced. Because the case may be heading for appeal, applicants

respectfully request a complete and proper rejection meeting the requirements of MPEP § 2112 or withdrawal of the rejection.

Claims 1-3, 9-12, 14-21, and 23-26 are rejected under 53 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,944,809 (Olarig). Applicants respectfully traverse this rejection for the following reasons.

In order to anticipate, the reference must identically disclose each claim element. In fact, Olarig does not identically disclose many of the recited claim elements.

The office action asserts that components 107 and 306 in Figure 4 of Olarig correspond to the recited scaleable node controllers. However, Olarig describes component 107 as a cache and component 306 as a local programmable interrupt controller (LOPIC). A cache and a LOPIC are not identical to a scaleable node controller.

In the Examiner's response to arguments, in numbered paragraph 56, the Examiner purports to answer applicants' prior traversal, but does so only selectively. Specifically, the Examiner does not answer and apparently concedes applicants' argument that the different terminology in fact describes different structure and functionality. The Examiner does not answer and apparently concedes applicants' argument that a cache has no relationship whatsoever in structure or functionality to a node controller. The Examiner does not answer and apparently concedes applicants' argument that with respect to the LOPIC 306, every 'controller' does not perform the same function as every other 'controller'. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a node controller performs a different function than an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a node controller has a different structure from an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that a node controller may have suitable structure to participate in an interrupt handling scheme, but an interrupt controller would not have suitable structure to perform the function of controlling a node of a multi-node system.

Applicants understand the Examiner's position to be that because the LOPIC 306 is a 'controller' and may have some connection to a 'node', it may read on the recited 'node controller'. Applicants submit that this interpretation is an unreasonably broad interpretation of the claim language and an incorrect reading of the reference. As the case appears to be heading for appeal, applicants respectfully request that the Examiner provide a reasoned response to the foregoing arguments in order to reduce issues for appeal. Applicants consider each unanswered argument as conceded for the purposes of appeal.

The office action asserts that component 312 in Figure 4 of Olarig corresponds to the recited scalability port switch. However, Olarig describes component 312 as a central programmable interrupt controller (COPIC). A COPIC is not identical to a scalability port switch.

In the Examiner's response to arguments, at numbered paragraph 56, the Examiner purports to answer applicants' prior traversal, but does so only selectively. Specifically, the Examiner does not answer and apparently concedes applicants' argument that the different terminology in fact describes different structure and functionality. The Examiner does not answer and apparently concedes applicants' argument that every controller does not perform the same function as every other controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a port switch performs a different function than an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a port switch has a different structure from an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that a port switch may have suitable structure to participate in an interrupt handling scheme, but an interrupt controller would not have suitable structure to perform the function of switching ports of a multi-node system. The Examiner does not answer and apparently concedes applicants' argument that in some applications a port switch may include structure to resolve node addresses and that the COPIC 312 appears to lack such structure.

Applicants understand the Examiner's position to be that because the COPIC 312 may be broadly considered as a 'switch' and may have some connection to a 'port', it may read on the recited 'port switch'. Applicants submit that this interpretation is an unreasonably broad interpretation of the claim language and an incorrect reading of the reference. As the case appears to be heading for appeal, applicants respectfully request that the Examiner provide a reasoned response to the foregoing arguments in order to reduce issues for appeal. Applicants consider each unanswered argument as conceded for the purposes of appeal.

Among other things, claim 1 further recites that the scalability port switch is to determine an address of one of said scaleable node controllers from said interrupt request. Olarig fails to teach or suggest this further recitation. In contrast to the present invention, Olarig describes a multi-processor system with LOPICs 306 connected to the COPIC 312 over the PIC bus 311. Olarig appears to function similarly to Tavallaei as discussed above. The Examiner has not identified (and applicants are unable to identify) any portion of Olarig that teaches or suggests that the LOPICs 306 have addresses associated therewith.

In the Examiner's response to arguments, at numbered paragraph 57, the Examiner has now clarified that the rejection relies on a theory of inherency. As noted in MPEP § 2112, the fact that a feature may be present in the reference is not sufficient to establish inherency. The Examiner has the burden of proving that the LOPIC 306 must have an address associated therewith. However, this is incorrect. Any of a number of schemes may be utilized for getting data to the appropriate processor 106. For example, the processor 106 in Olarig may include a processor ID and the message on the bus 311 may include the processor ID (e.g. similarly to Tavallaei as discussed above). Olarig expressly describes that the LOPIC maintains a register with the processor ID and the processor ID is used for delivering interrupts (see col. 7, lines 46-51). Because the data delivery scheme in Olarig might not use an address for the LOPIC 306, the reliance on inherency (and the rejection) fails.

Because Olarig fails to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claim 1 is not

anticipated by Olarig, and is patentable over Olarig. Claims 2-3 depend from claim 1 and are likewise patentable.

With respect to claims 9 and 18, for the reasons given above Olarig does not disclose the recited scaleable node controller, the recited scalability port switch, or the recited address of the scaleable node controller. Accordingly, claim 9 and its dependent claims 10-12 and 14-17 are not anticipated by and are patentable over Olarig. Likewise, claim 18 and its dependent claims 19-21 and 23-26 are patentable over Olarig.

With respect to claims 11 and 20, the office action identifies col. 10, lines 8-10 for the recited comparing a priority of the interrupt request with a priority of the processor. In the Examiner's response to arguments, in numbered paragraph 61, the Examiner further identifies col. 3, lines 4-7 for this recitation. Col. 3, lines 4-7 discusses only comparing the priority of the interrupt with priorities of other tasks. Col. 10, lines 8-10 (which has no connection with the other cited portion of col. 3, lines 4-7) discusses only comparing a processor task priority level with other processors to select the least busy processor. However, neither cited portion makes any reference whatsoever to comparing a priority of the interrupt request with a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Olarig.

In numbered paragraph 58, the Examiner relies on page 8, lines 16-17 of the present specification to improperly read limitations from the specification into the claims. The Examiner is respectfully directed to page 5, lines 25-27 of the present specification.

Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,119,191 (Neal). Applicants respectfully traverse this rejection for the following reasons.

Neal fails to make up for the above-noted deficiencies in Tavallaei. Accordingly, the office fails to establish a prima facie case of obviousness.

Moreover, claim 4 recites a first input/output hub coupled between the peripheral component interconnect bus and the first scalability port switch, wherein said first input/output hub is able to support a plurality of additional peripheral component interconnect hubs. The office action asserts that component 28 corresponds to the recited hub. However, component 28 is simply described as an ASIC connected to a PCI bus, not an I/O hub. In fact, the word "hub" cannot be found in Tavallaei. No one skilled in the art would be motivated to replace the ASIC 28 of Tavallaei with the hubs described in Neal.

In numbered paragraph 59, the Examiner yet again fails to give different terminology any relevance, even though the different terms in fact refer to different structures. One of ordinary skill in the art would appreciate that the ASIC 28 does not necessarily have the same structure or perform the same function as an I/O hub, just because it 'has inputs and outputs'.

Because the office action fails to establish a prima facie case of obviousness and because the ASIC 28 is not an I/O hub, claim 4 is patentable over Tavallaei in view of Neal. Claim 5 depends from claim 4 and is likewise patentable.

Claims 6 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei, in view of Neal, and further in view of Intel's Multiprocessor Specification, dated May 1997 (MP). Applicants respectfully traverse this rejection for the following reasons.

Neal and MP both fail to make up for the above-noted deficiencies in Tavallaei. Accordingly, the office fails to establish a prima facie case of obviousness. Claim 6 and 7 depend from claim 5, and are accordingly patentable for the reasons given above. Claims 6 and 7 are further patentable for the following reasons.

Claim 6 recites that the first pair of scaleable node controllers and the second pair of scaleable node controllers are coupled to a second scalability port switch. Claim 7 depends from claim 6 and further recites that the second scalability port switch is coupled to the first input/output hub.

Because the office fails to establish a prima facie case of obviousness and because Olarig does not teach or suggest two pair of scaleable node controllers with each pair connected to two different scalability port switches, claims 6 and 7 are separately patentable over Tavallaei in view of Neal and further in view of Olarig.

Claims 13 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,189,065 (Arndt). Claims 13 and 22 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Olarig in view of Arndt. Applicants respectfully traverse these rejections for the following reasons.

Arndt fails to make up for the above noted deficiencies in Tavallaei and Olarig. Accordingly, the office action fails to establish a prima facie case of obviousness. For the Examiner's convenience, the claim language, the Examiner's stated rejection, and the cited portion of Arndt are reproduced below:

Claims 13 and 22	... wherein said scalable node controller redirects the interrupt request through the scalability port switch to a different processor.
Examiner's rejection	... Arndt discloses redirecting an interrupt to a different processor. Therefore it would have been obvious to combine the teachings of Arndt and [the primary reference] to redirect an interrupt to different processor since ...
Claim 8 Of Arndt	... an offload selector for offloading said interrupt message to a second processor if said first processor is busy servicing another interrupt signal ...

The claim language does not recite 'redirect an interrupt to a different processor'. The claim language recites that the scaleable node controller redirects the interrupt request through the scalability port switch to a different processor. The office action completely fails to address several of the claim recitations, and accordingly fails to establish a prima facie case of obviousness. The Examiner's response to arguments, in numbered paragraph 60, fails to clarify or explain the Examiner's position or answer applicants' previous traversal. In any event, the cited portion of Arndt is silent in regard to these claim recitations.

Because the Arndt fails to make up for the respective deficiencies in Tavallaei and Olarig, and because there is no motivation to combine the references as suggested by the

office action, and because the Examiner fails to establish a prima facie case of obviousness, and because the cited portion of Arndt fails to describe that a scalable node controller redirects the interrupt request through a scalability port switch to a different processor, claims 13 and 22 are separately patentable over the cited combination of references.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

February 21, 2006
Date

/Paul E. Steiner/
Paul E. Steiner
Reg. No. 41,326
(703) 633-6830

Intel Americas, Inc., LF3
4030 Lafayette Center Drive
Chantilly, VA 20151